NTP45N06, NTB45N06

Power MOSFET 45 Amps, 60 Volts

N–Channel TO–220 and D2PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter V_{SD} Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	60	Vdc
Drain–to–Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	60	Vdc
Gate–to–Source Voltage – Continuous – Non–Repetitive ($t_p \le$ 10 ms)	 V_{GS} V_{GS}	 ±20 ±30	Vdc
Drain Current – Continuous @ T_A = 25°C – Continuous @ T_A = 100°C – Single Pulse ($t_p \le$ 10 µs)	 I_D I_D I_{DM}	 45 30 150	 Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1.) Total Power Dissipation @ T_A = 25°C (Note 2.)	P_D	125 0.83 3.2 2.4	W W/°C W W
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to +175	°C
Single Pulse Drain–to–Source Avalanche Energy – Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vdc, RG = 25 Ω, $I_{L(pk)}$ = 40 A, L = 0.3 mH, V_{DS} = 60 Vdc)	E_{AS}	240	mJ

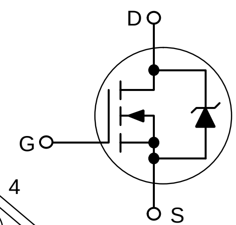
1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in^2).

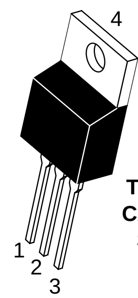
ON Semiconductor™

http://onsemi.com

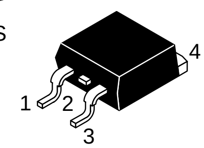
45 AMPERES
60 VOLTS
$R_{DS(on)}$ = 26 mΩ

N–Channel



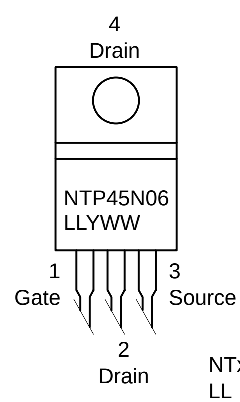


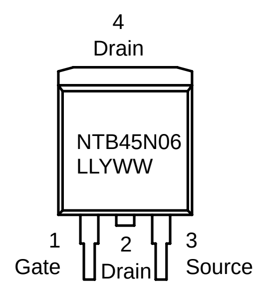
TO–220AB CASE 221A STYLE 5



D2PAK CASE 418B STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS





NTx45N06	= Device Code	
LL	= Location Code	
Y	= Year	
WW	= Work Week	

ORDERING INFORMATION

Device	Package	Shipping
NTP45N06	TO–220AB	50 Units/Rail
NTB45N06	D^{2}PAK	50 Units/Rail
NTB45N06T4	D^{2}PAK	800/Tape & Reel

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Thermal Resistance – Junction–to–Case – Junction–to–Ambient (Note 3.) – Junction–to–Ambient (Note 4.)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.2 46.8 63.2	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain–to–Source Breakdown Voltage (Note 5.) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 –	 70 57	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	–	–	±100	nAdc
ON CHARACTERISTICS (Note 5.)						
Gate Threshold Voltage (Note 5.) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 2.0 –	 2.8 7.2	 4.0 –	Vdc mV/°C
Static Drain–to–Source On–Resistance (Note 5.) (V_{GS} = 10 Vdc, I_D = 22.5 Adc)		$R_{DS(on)}$	 –	 21	 26	mOhm
Static Drain–to–Source On–Voltage (Note 5.) (V_{GS} = 10 Vdc, I_D = 45 Adc) (V_{GS} = 10 Vdc, I_D = 22.5 Adc, T_J = 150°C)		$V_{DS(on)}$	 – –	 0.93 0.93	 1.4 –	Vdc
Forward Transconductance (Note 5.) (V_{DS} = 8.0 Vdc, I_D = 12 Adc)		g_{FS}	–	16.6	–	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	–	1224	1725	pF
Output Capacitance		C_{oss}	–	345	485	
Transfer Capacitance		C_{rss}	–	76	160	
SWITCHING CHARACTERISTICS (Note 6.)						
Turn–On Delay Time	(V_{DD} = 30 Vdc, I_D = 45 Adc, V_{GS} = 10 Vdc, R_G = 9.1 Ω) (Note 5.)	$t_{d(on)}$	–	10	25	ns
Rise Time		t_r	–	101	200	
Turn–Off Delay Time		$t_{d(off)}$	–	33	70	
Fall Time		t_f	–	106	220	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 45 Adc, V_{GS} = 10 Vdc) (Note 5.)	Q_T	–	33	46	nC
		Q_1	–	6.4	–	
		Q_2	–	15	–	
SOURCE–DRAIN DIODE CHARACTERISTICS						
Forward On–Voltage	(I_S = 45 Adc, V_{GS} = 0 Vdc) (Note 5.) (I_S = 45 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	– –	1.08 0.93	1.2 –	Vdc
Reverse Recovery Time	(I_S = 45 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 5.)	t_{rr}	–	53.1	–	ns
		t_a	–	36	–	
		t_b	–	16.9	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.087	–	μC

3. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in^2).
4. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in^2).
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

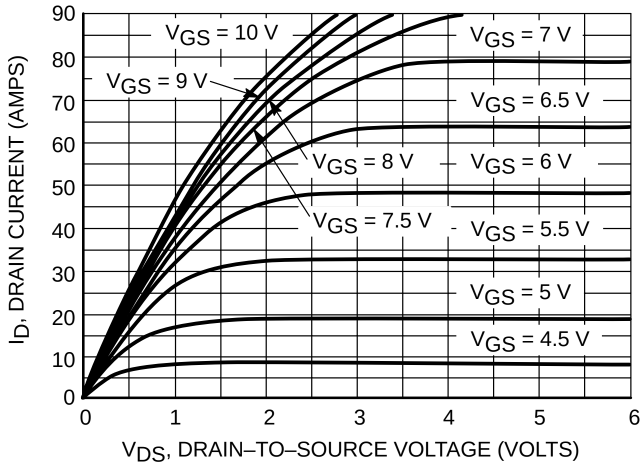


Figure 1. On–Region Characteristics

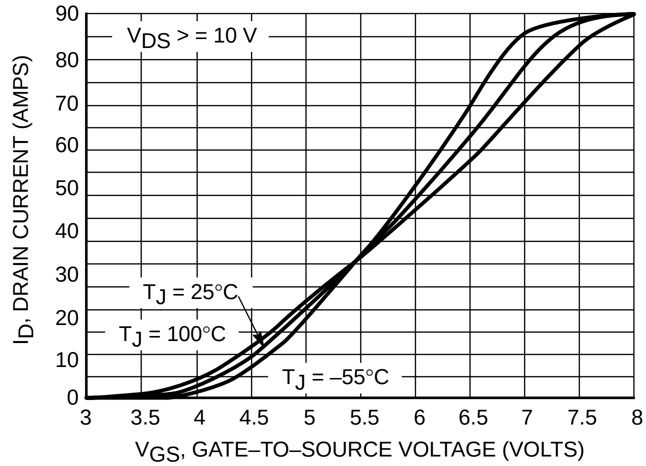


Figure 2. Transfer Characteristics

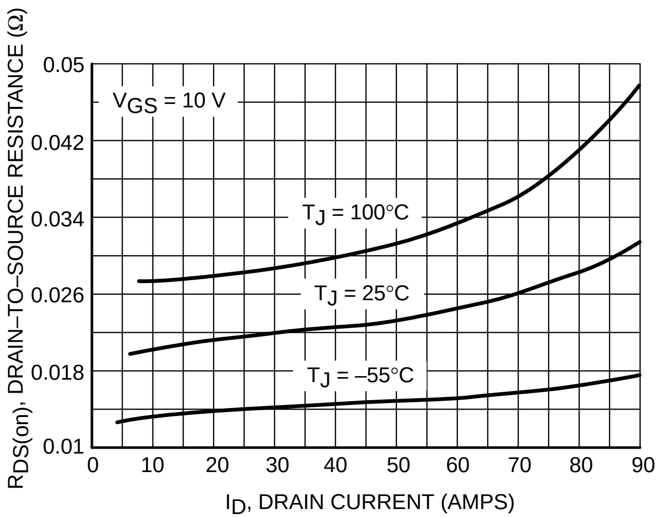


Figure 3. On–Resistance vs. Gate–to–Source Voltage

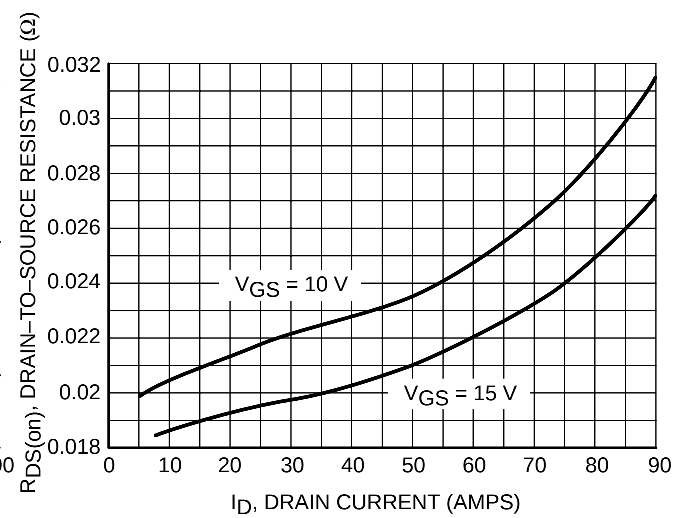


Figure 4. On–Resistance vs. Drain Current and Gate Voltage

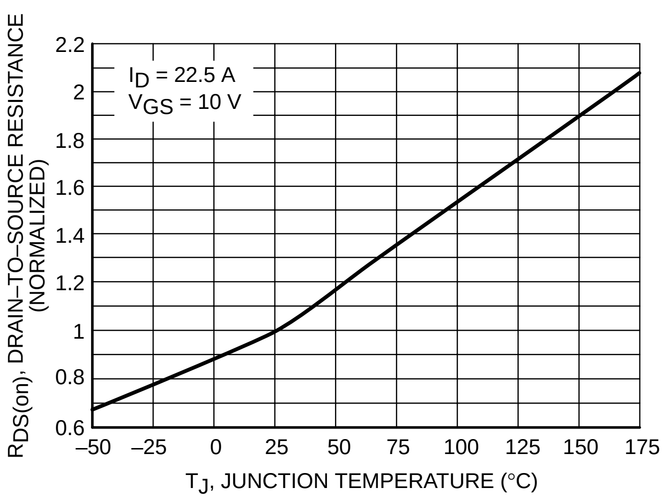


Figure 5. On–Resistance Variation with Temperature

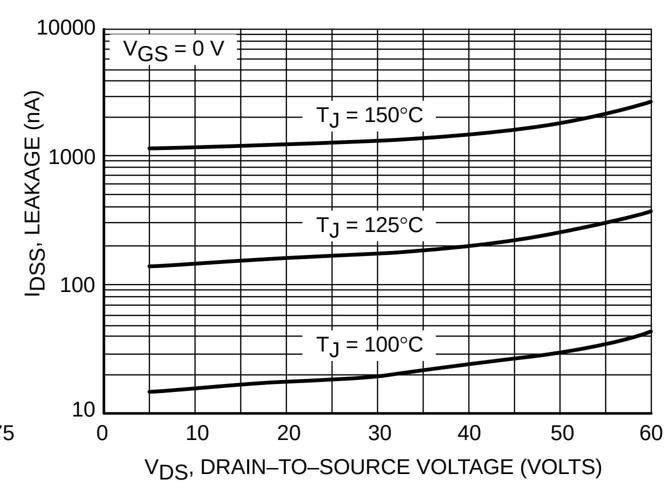


Figure 6. Drain–to–Source Leakage Current vs. Voltage

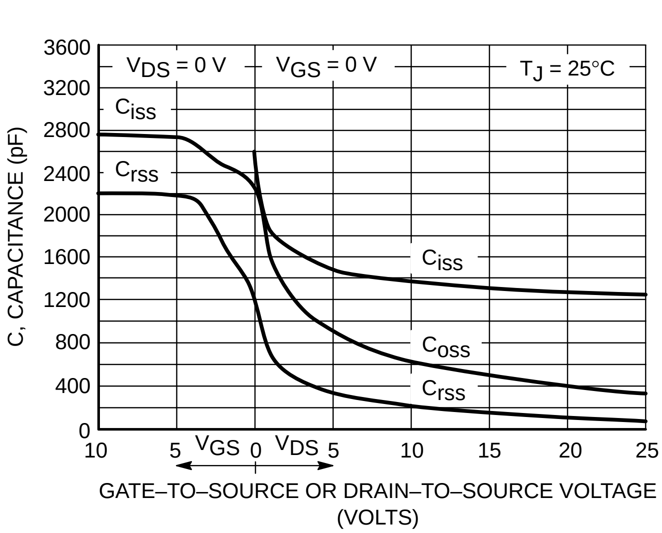


Figure 7. Capacitance Variation

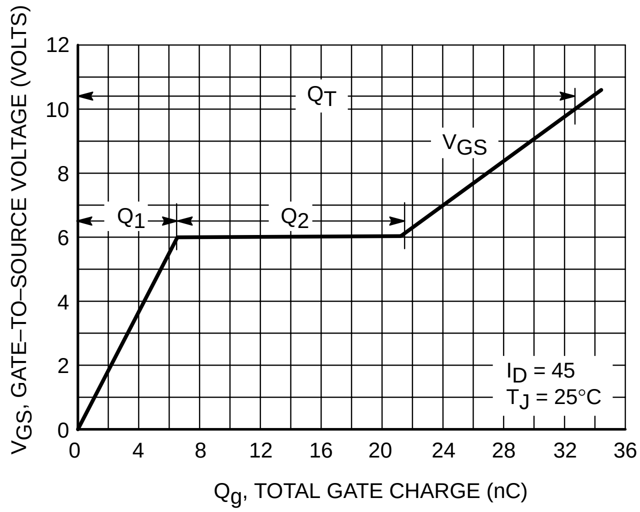


Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

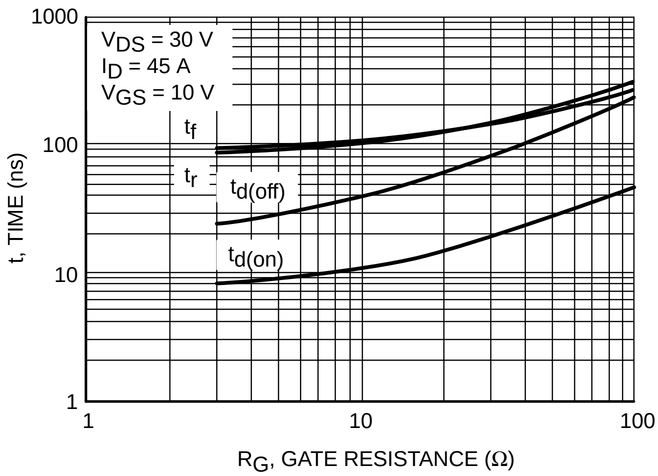


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

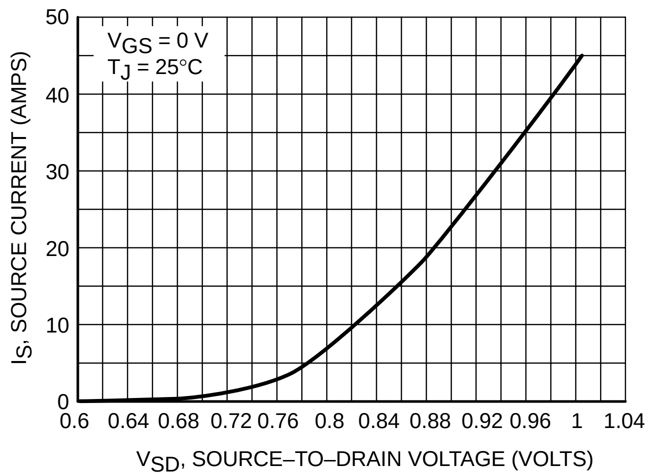


Figure 10. Diode Forward Voltage vs. Current

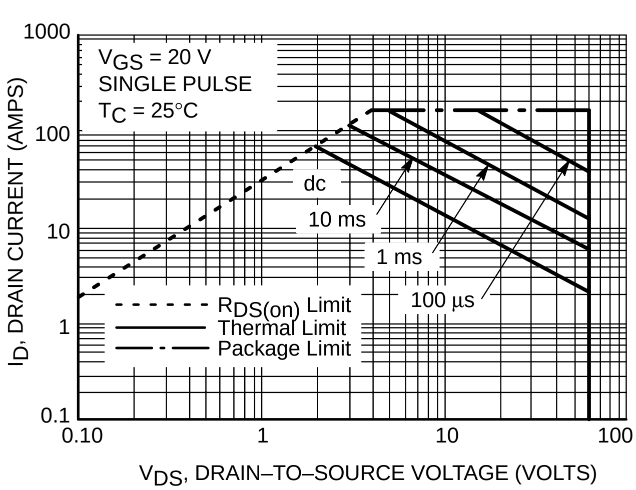


Figure 11. Maximum Rated Forward Biased Safe Operating Area

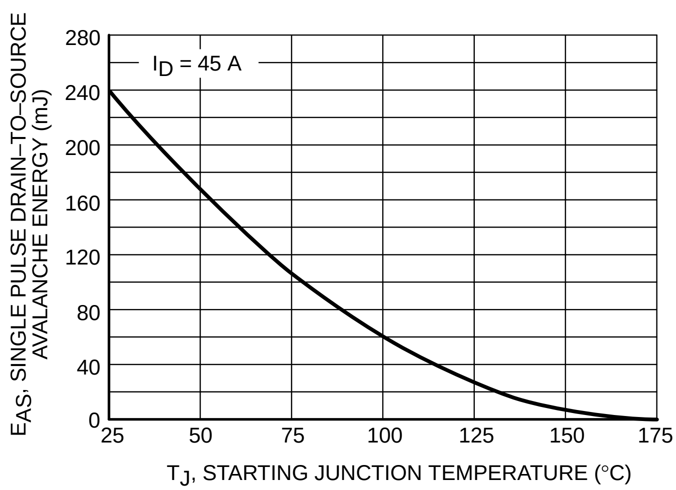


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

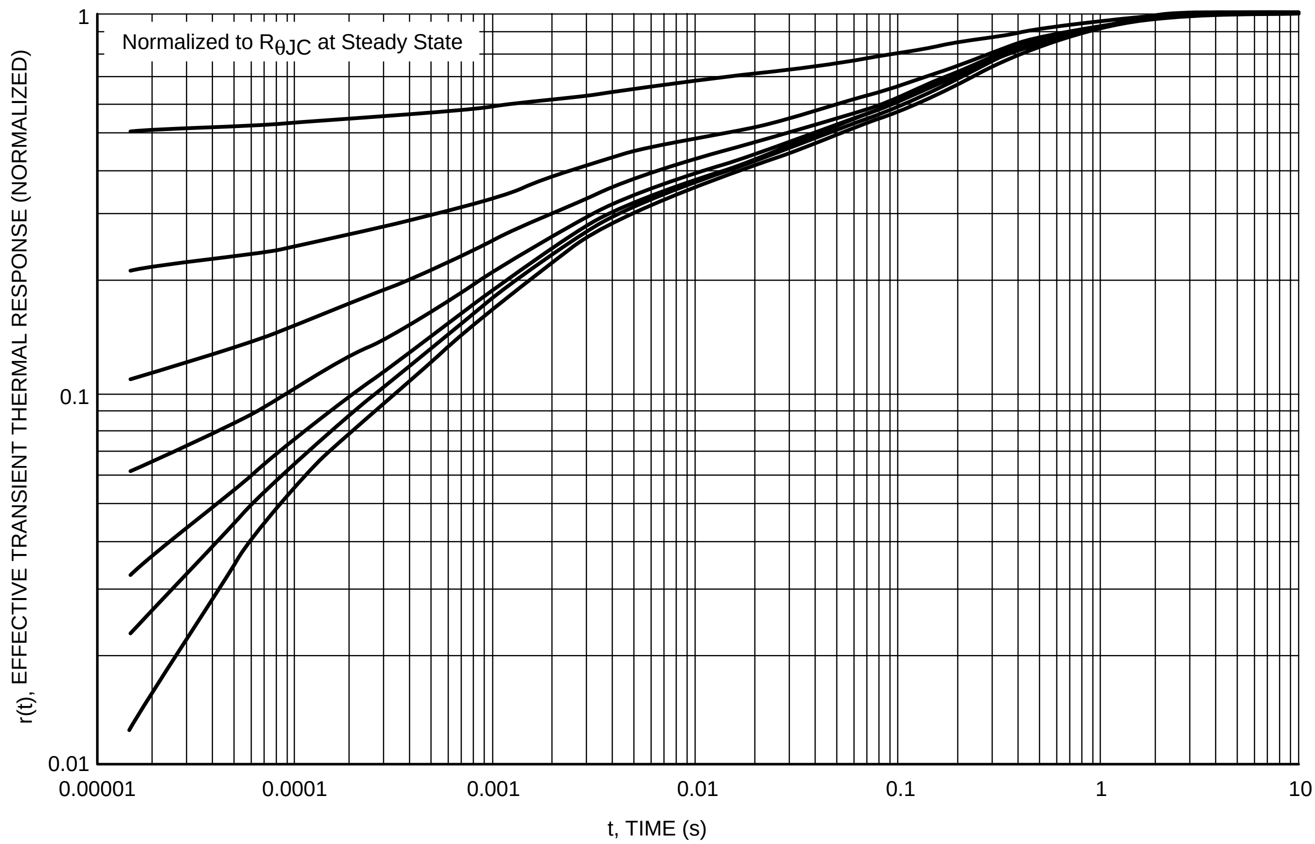


Figure 13. Thermal Response

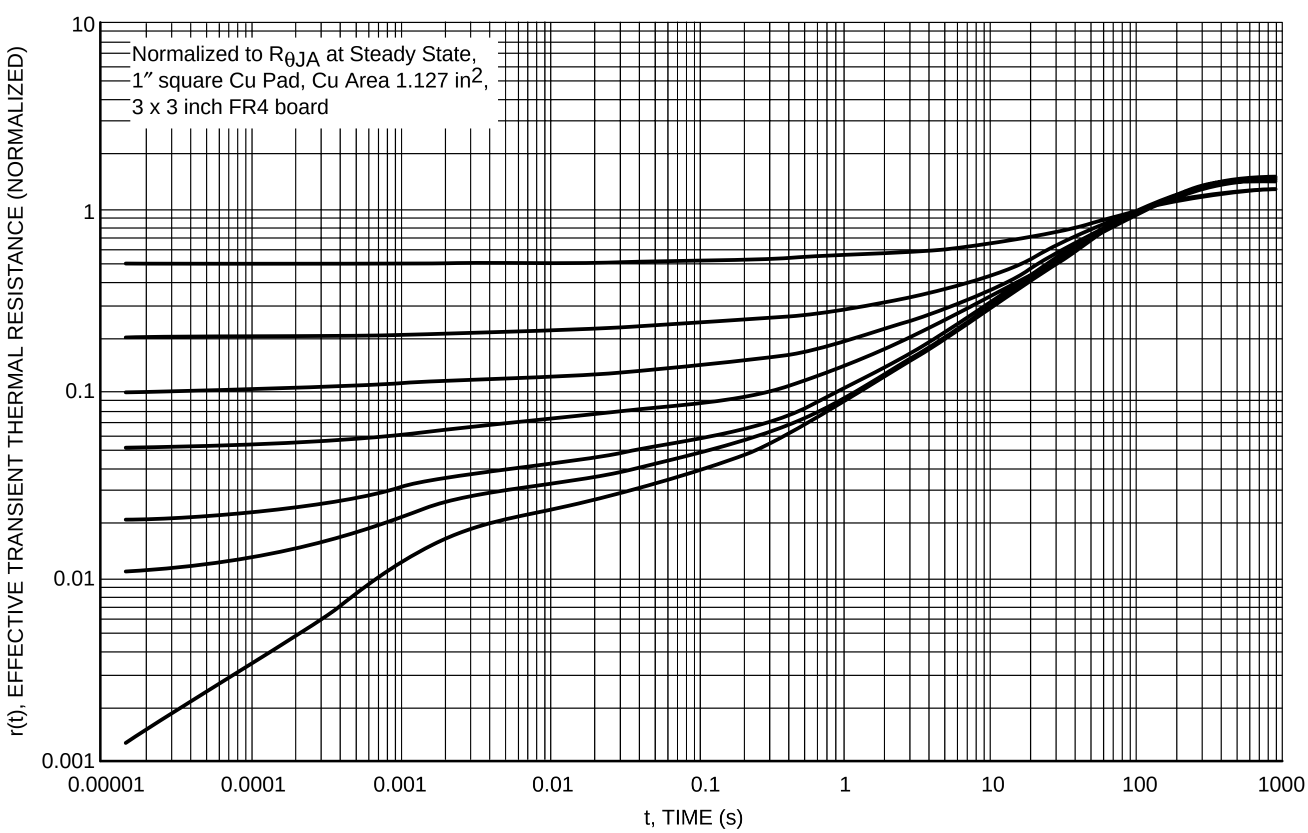
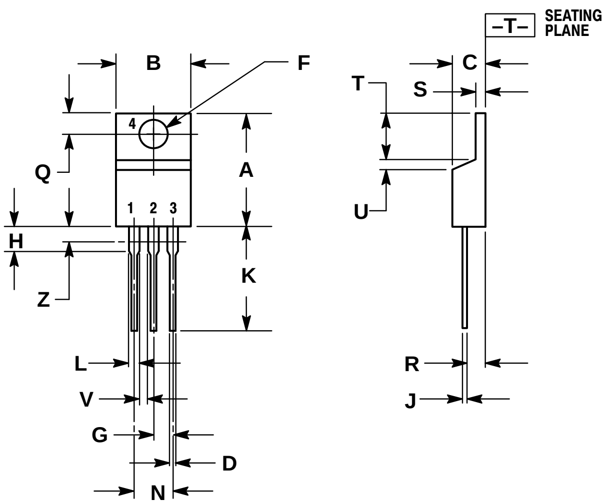


Figure 14. Thermal Response

PACKAGE DIMENSIONS

TO–220 THREE–LEAD
TO–220AB
CASE 221A–09
ISSUE AA



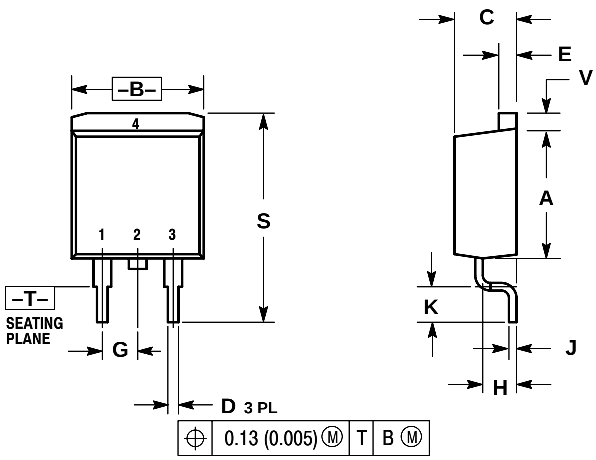
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PACKAGE DIMENSIONS

D2PAK
CASE 418B–03
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
Fax: 303–675–2176 or 800–344–3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303–675–2167 or 800–344–3810 Toll Free USA/Canada

N. American Technical Support: 800–282–9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support
German Phone: (+1) 303–308–7140 (Mon–Fri 2:30pm to 7:00pm CET)
Email: ONlit–german@hibbertco.com
French Phone: (+1) 303–308–7141 (Mon–Fri 2:00pm to 7:00pm CET)
Email: ONlit–french@hibbertco.com
English Phone: (+1) 303–308–7142 (Mon–Fri 12:00pm to 5:00pm GMT)
Email: ONlit@hibbertco.com

EUROPEAN TOLL–FREE ACCESS*: 00–800–4422–3781
*Available from Germany, France, Italy, UK, Ireland

CENTRAL/SOUTH AMERICA:
Spanish Phone: 303–308–7143 (Mon–Fri 8:00am to 5:00pm MST)
Email: ONlit–spanish@hibbertco.com
Toll–Free from Mexico: Dial 01–800–288–2872 for Access – then Dial 866–297–9322

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support
Phone: 303–675–2121 (Tue–Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001–800–4422–3781
Email: ONlit–asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4–32–1 Nishi–Gotanda, Shinagawa–ku, Tokyo, Japan 141–0031
Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local
Sales Representative.